CPC9909
High Efficiency, Off-Line, High Brightness LED Driver

Features

- $8V_{DC}$ to $550V_{DC}$ Input Voltage Range
- >90% Efficiency
- Stable Operation at >50% Duty Cycle
- Drives Multiple LEDs in Series/Parallel
- Regulated LED Current
- Linear or PWM Brightness Control Inputs
- Resistor-Programmable Minimum Off-Time
- SOIC-8 RoHS Compliant Package
- Buck or Boost Configuration

Applications

- Flat-Panel Display RGB Backlighting
- Signage and Decorative LED Lighting
- DC/DC or AC/DC LED Driver Applications

Description

The CPC9909 is a low cost, high-efficiency, offline, high-brightness (HB) LED driver manufactured using Clare's high voltage BCDMOS on SOI process. This driver has an internal regulator that allows it to operate from $8V_{DC}$ to $550V_{DC}$. This wide input operating voltage range enables the driver to be used in a broad range of HB LED applications.

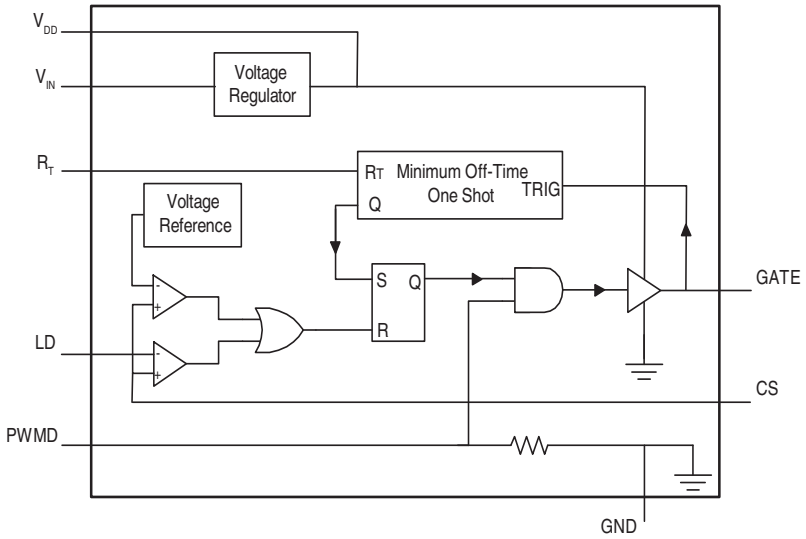
The CPC9909 features pulse frequency modulation (PFM) with a constant peak-current control scheme. This regulation scheme is inherently stable, allowing the driver to be operated above 50% duty cycle without open loop instability or sub-harmonic oscillations. LED dimming can be implemented by applying a small DC voltage to the LD pin, or by applying a low frequency PWM signal to the PWMD pin.

The CPC9909 is available in a standard 8-lead SOIC package and a thermally enhanced 8-lead SOIC package with an exposed thermal pad (EP).

Ordering Information

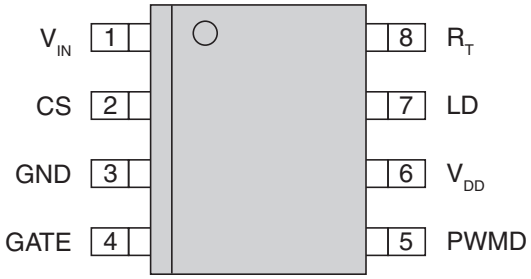
Part	Description
CPC9909N	SOIC-8 (100/Tube)
CPC9909NTR	SOIC-8 Tape & Reel (2000/Reel)
CPC9909NE	SOIC-8 EP (Exposed Pad) (100/Tube)
CPC9909NETR	SOIC-8 EP (Exposed Pad)Tape & Reel (2000/Reel)

CPC9909 Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Description
1	V_{IN}	Input voltage
2	CS	LED Current Sense input. Internal current sense threshold is set at $V_{CS(high)}$. The external sense resistor sets the maximum LED current.
3	GND	Device Ground
4	GATE	External MOSFET gate driver output
5	PWMD	Low-frequency PWM dimming control input with internal pull-down resistor.
6	V_{DD}	Regulated supply voltage output. Requires a storage capacitor to GND. Can be overdriven by external voltage applied to V_{DD} .
7	LD	Linear Dimming. Apply a voltage less than $V_{CS(high)}$ to dim the LED(s).
8	R_T	Resistor to GND sets the minimum off-time.
EP	-	Electrical and thermal conductive pad on the bottom of CPC9909NE. Connect this pad to ground and provide sufficient thermal coupling to remove heat from the package.

1.3 Absolute Maximum Ratings

Parameter	Symbol	Maximum	Unit
Input Voltage to GND	V_{IN}	-0.5 to +560	V
Inputs and Outputs Voltage to GND	CS, LD, PWMD, GATE	-0.3 to V_{DD}+0.3	V
V_{DD} , Externally Applied	$V_{DD.EXT}$	15	V
Power Dissipation:			
SOIC-8 With Thermal Tab	P_D	2.5	W
SOIC-8 W/O Thermal Tab		0.975	W
Junction Temperature, Operating	T_J	-55 to +150	°C
Operating Temperature	T_A	-55 to +85	°C
Storage Temperature	T_{STG}	-55 to +150	°C

Electrical absolute maximum ratings are at 25°C.

Absolute maximum ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Input Voltage Range	V_{IN}	12	-	550	V_{DC}
PWMD Frequency	f_{PWMD}	-	500	-	Hz
Operating Temperature	T_A	-40	-	+85	°C

1.5 Electrical Characteristics

Unless otherwise specified, all electrical specifications are provided for T_A=25°C.

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input						
Input Voltage Range	DC Input Voltage	V_{IN}	8	-	550	V_{DC}
Shut-Down Mode Supply Current	V_{IN}=8 to 550V, PWMD to GND	I_{IN}	-	0.3	0.6	mA
Regulator						
Voltage Regulator Output	V_{IN}=15V to 550V, I_{DD}=0, I_{GATE}=0	V_{DD}	7.2	7.8	8.4	V_{DC}
V_{DD} Current Available for External Circuitry	-	I_{DD}	-	-	2	mA
V_{DD} Load Regulation	V_{IN}=15V, I_{DD}=1mA	ΔV_{DD}	-	150	200	mV
PWM Dimming						
PWMD Input Low Voltage	V_{IN}=8V to 550V	$V_{PWMD(low)}$	-	-	0.5	V
PWMD Input High Voltage	V_{IN}=8V to 550V	$V_{PWMD(high)}$	2.4	-	-	
PWMD Pull-Down Resistance	-	R_{PWMD}	80	115	150	kΩ
Current Sense Comparator						
Current Sense Input Current						µA
Input Low	CS=0V	I_{IL}	-5	-	5	
Input High	CS=V_{DD}	I_{IH}	-5	0	5	
Current Sense Threshold Voltage	-40°C ≤ T_A ≤ 85°C, V_{IN}=15V to 550V	$V_{CS(high)}$	200	250	300	mV
	-55°C ≤ T_A < -40°C, V_{IN}=15V to 550V		180	-	300	
Current Sense Blanking Interval	R_T=400kΩ	t_{BLANK}	-	400	-	ns
Delay from CS Trip to Gate Low	R_T=400kΩ	t_{DELAY}	-	300	-	ns
Minimum Off-Time One-Shot						
Minimum Off-Time	R_T=400kΩ	t_{off}	6	-	8	µs
Gate Driver						
Gate High Output Voltage	I_{OUT}=-10mA	$V_{GATE(high)}$	V_{DD}-0.3	V_{DD}-0.06	-	V
Gate Low Output Voltage	I_{OUT}=+10mA	$V_{GATE(low)}$	-	0.03	0.3	
Gate Output Rise Time	C_{GATE}=500pF	t_{RISE}	-	16	-	ns
Gate Output Fall Time	C_{GATE}=500pF	t_{FALL}	-	7	-	

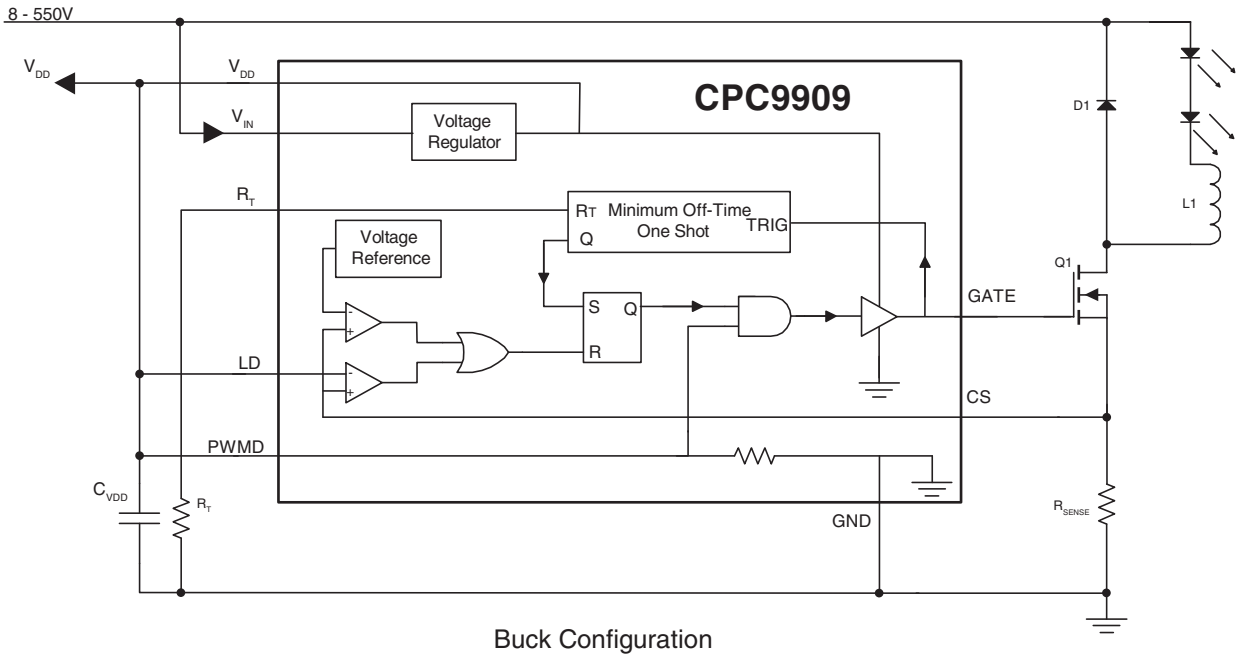
1.6 Thermal Characteristics

Parameter	Package	Symbol	Minimum	Typical	Maximum	Unit
Thermal Resistance, Junction-to-Ambient	SOIC-8 With Thermal Pad (NE) [1]	$R_{\theta JA}$	-	50	-	°C/W
	SOIC-8 W/O Thermal Pad (N)		-	128	-	

[1] Use of a four-layer PCB can improve thermal dissipation (reference EIA/JEDEC JESD51-5).

2. Functional Description

Figure 1 Typical Application Circuit



Buck Configuration

2.1 Overview

The CPC9909 drives the LEDs via a minimum off-time, peak-current-limited, pulse-frequency modulation scheme. This control scheme is inherently stable, and the driver can be operated above a 50% duty cycle without any open-loop instability or sub-harmonic oscillations. Since the switching frequency depends on the LED load current, it results in a high efficiency operation.

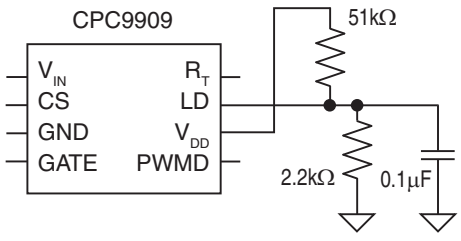
2.2 LED Driver Theory of Operation

The typical application circuit is as shown in **Figure 1** When PWMD is high, the control circuit is enabled and the gate driver turns on the external power MOSFET (Q1), causing the inductor (L1) current to ramp up until the voltage across the current sense resistor (R_{SENSE}) exceeds $V_{CS(high)}$. When the voltage at the CS pin exceeds this threshold, the gate driver turns Q1 off. Q1 remains off for the duration of the fixed minimum off-time. While the switch is off, the inductor continues to deliver the current to the load though the diode (D1). When the off-time expires, Q1 turns on again until the peak current limit is reached, and the process repeats.

The peak current limit threshold is set by the external sense resistor, R_{SENSE}, and the internal voltage threshold, $V_{CS(high)}$. This internal voltage threshold can also be set externally via the LD pin. The lower of these two thresholds and R_{SENSE} set the peak current in the inductor.

A soft start function can be implemented by ramping up the DC voltage at the LD pin from 0V to $V_{CS(high)}$ at the desired rate. To utilize the soft start function, connect a resistor divider from V_{DD} to ground and a capacitor from the LD pin to ground, as shown in

Figure 2 Soft-Start Circuit



2.3 Input Voltage Regulator

The CPC9909 has an internal voltage regulator that can work with input voltages ranging from $12V_{DC}$ to $550V_{DC}$. When a DC voltage greater than 12V is applied at the V_{IN} pin, the internal voltage regulator regulates the voltage down to a typical 7.8V. The V_{DD} pin is the internal voltage regulator output pin and must be bypassed by a low-ESR capacitor to provide a low impedance path for high frequency switching noise.

The CPC9909 driver does not require the bulky start-up resistors typically needed for off-line controllers. The internal voltage regulator provides sufficient voltage and current to power internal IC circuits. This voltage is also available at the V_{DD} pin, and can be used as a bias voltage for external circuitry.

The internal voltage regulator can be bypassed by applying an external DC voltage to the V_{DD} pin that is slightly higher than the internally generated regulator voltage. This reduces the power dissipation of the integrated circuit, and it is more suitable in isolated applications where an auxiliary winding can be used to drive the V_{DD} pin.

The total input current drawn from the V_{IN} pin is equal to the quiescent current drawn by the internal circuitry (which is specified at 0.6mA maximum) plus the gate driver current. See “Shut-Down Mode Supply Current” in **Section 1.5 “Electrical Characteristics” on page 4**.

The current draw of the gate driver depends on the switching frequency and the gate charge of the external power MOSFET. The total input current can be calculated by:

$$I_{IN} \approx 0.6mA + (Q_{GATE} \times f_S)$$

Where Q_{GATE} is the total gate charge of the MOSFET and f_S is the oscillator external frequency.

2.4 Current Sense Resistor

The peak LED current is set by an external sense resistor (R_{SENSE}) connected from the CS pin to ground.

The value of the current sense resistor is calculated based on the average LED current desired, the current sense threshold, and the inductor ripple current.

The peak-to-peak difference in the inductor current waveform is referred to as inductor ripple current (the inductor is typically selected to be large enough to keep this ripple within 30% of the average). Factor in the ripple current when calculating the sense resistor.

The current sense resistor value can be found by:

$$R_{SENSE} = \frac{V_{CS(high)}}{I_{LED} + 0.5\Delta I_L}$$

Where:

- $V_{CS(high)}$ = current sense threshold =0.25V (or V_{LD})
- I_{LED} = average LED/inductor current
- ΔI_L = inductor ripple current = $0.3*I_{LED}$

Combining terms:

$$R_{SENSE} = \frac{V_{CS(high)}}{1.15 \bullet I_{LED}}$$

2.5 Current Sense Blanking

The CPC9909 has an internal current sense blanking circuit. When the power MOSFET is turned on, the external inductor can cause an undesired spike at the current sense pin, initiating a premature termination of the gate pulse. To avoid this condition, a typical 400ns internal leading edge blanking time is implemented, thereby eliminating the need for external RC filtering, and simplifying the design. During the current sense blanking time, the current limit comparator is disabled, preventing the gate-drive circuit from terminating the gate-drive signal.

2.6 Enable/Disable Function

Connecting the PWMD pin to V_{DD} enables the gate driver. Connecting PWMD to GND disables the gate driver and sets the device in standby mode. In standby mode, the quiescent current is 0.6mA maximum.

2.7 Minimum Off-Time One-Shot

The CPC9909 uses a fixed off-time control scheme. The minimum off-time is set by an external resistor connected between the RT and GND terminals.

The off-time can be determined by:

$$t_{off}(\mu s) = \{[(R_T(k\Omega))/66] + 0.8\}$$

Off-time selection indirectly determines the switching frequency of the LED driver.

The switching frequency is determined by:

$$F_S = \frac{1 - D}{t_{off}}$$

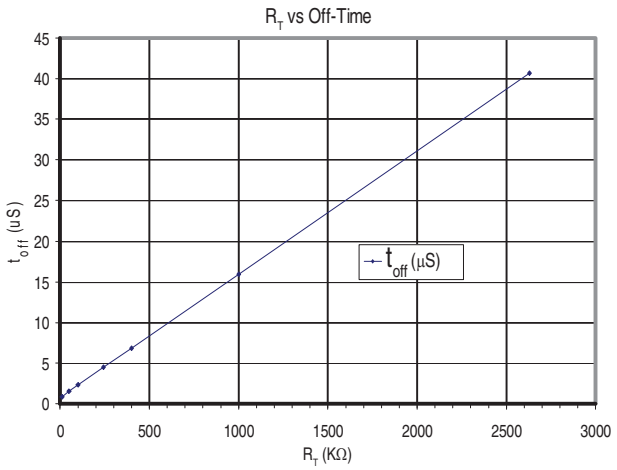
Where:

- D = duty cycle
- t_{off} = Off-time

In general, switching frequency selection is based on the inductor size, controller power dissipation, and the input filter capacitor.

The typical off-line LED driver switching frequency, f_S, is between 30 kHz and 120 kHz.

This operating range gives the designer a reasonable compromise between switching losses and inductor size. The internal off-time one-shot has an accuracy of ±20%. The figure below shows the R_T resistor selection for the desired off-time.



2.8 Inductor Design

The inductor value is defined by the LED/inductor ripple current, minimum off time, and the output voltage. The minimum off time is determined by the duty cycle and switching frequency. The duty cycle is given by:

$$D = \frac{V_{LEDstring}}{V_{in(min)}}$$

Where:

- $V_{LEDstring}$ is the LED string voltage at the desired average LED current.
- $V_{in(min)}$ is the minimum DC input voltage.

The minimum inductor value for a given ripple current is:

$$L_{MIN} = \left[\frac{V_{LEDstring}}{\Delta I_L}\right] \times t_{off}$$

Where:

- ΔI_L = Ripple Current

The inductor peak current is given by:

$$I_{LPeak} = I_{LED} + 0.5\Delta I_L$$

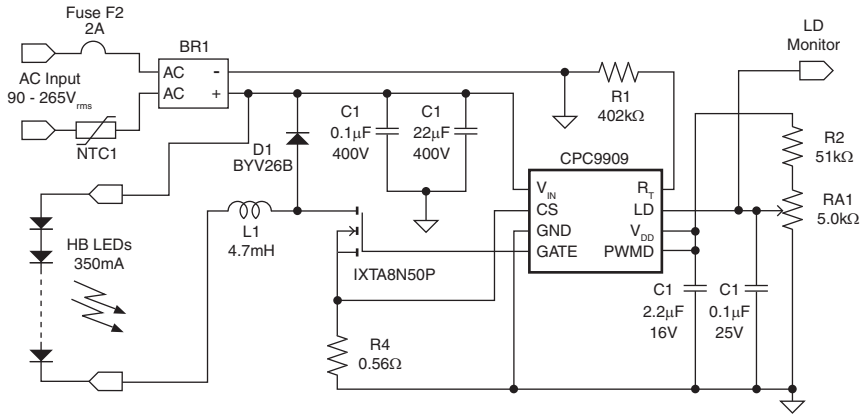
2.9 Gate Output Drive

The CPC9909 uses an internal gate drive circuit to turn on and off an external power MOSFET. The gate driver can drive a variety of MOSFETs. For a typical off-line application, the total MOSFET gate charge will be less than 25nC.

2.10 Linear Dimming

A linear dimming function can be implemented by applying a DC control voltage to the LD pin. By varying this voltage from 0V to $V_{CS(high)}$, the user can adjust the current level in the LEDs which in turn will increase or decrease the light intensity. The control voltage to the LD pin can be generated from an external voltage divider network from V_{DD}. This function is useful if the user requires LED current of a particular level, and there is no exact R_T value available. Note that applying a voltage higher than the current sense threshold voltage to the LD pin will not change the output current due to the fixed internal threshold setting. When the LD pin is not used, it should be connected to V_{DD}.

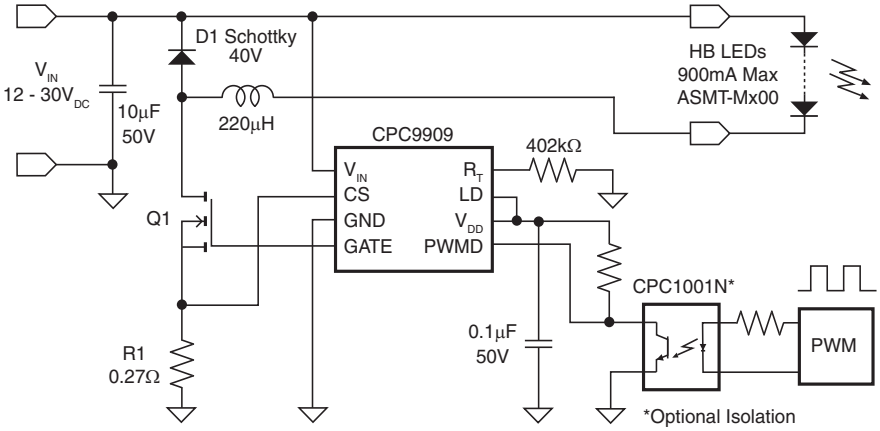
Figure 3 Typical Linear Dimming Application Circuit



2.11 PWM Dimming

Pulse width modulation dimming can be implemented by driving the PWMD pin with a low frequency square wave signal in the range of a few hundred Hertz. The PWMD signal controls the LED brightness by gating the PWM gate driver output pin GATE. The signal can be generated by a microcontroller or a pulse generator with a duty cycle proportional to the amount of desired light output.

Figure 4 Buck Driver for PWM Dimming Application Circuit



2.12 Combination Linear and PWM Dimming

A combination of linear and PWM dimming techniques can be used to achieve a large dimming ratio.

3. Manufacturing Information

3.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Clare classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL) rating** as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Rating
CPC9909N / CPC9909NE	MSL 1

3.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

3.3 Reflow Profile

This product has a maximum body temperature and time rating as shown below. All other guidelines of **J-STD-020** must be observed.

Device	Maximum Temperature x Time
CPC9909N / CPC9909NE	260°C for 30 seconds

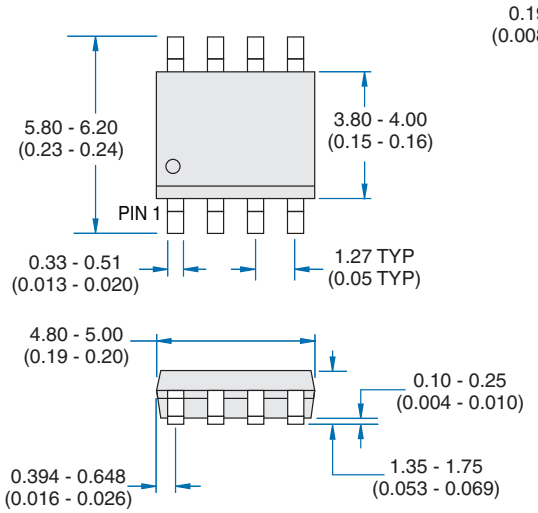
3.4 Board Wash

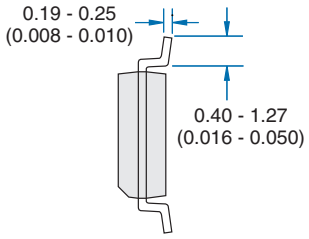
Clare recommends the use of no-clean flux formulations. However, board washing to remove flux residue is acceptable, and the use of a short drying bake may be necessary. Chlorine-based or Fluorine-based solvents or fluxes should not be used. Cleaning methods that employ ultrasonic energy should not be used.

3.5 Mechanical Dimensions

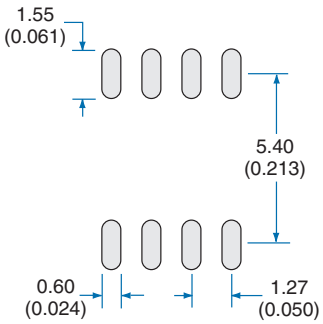
3.5.1 8-Pin SOIC Package

8-Pin SOIC Package





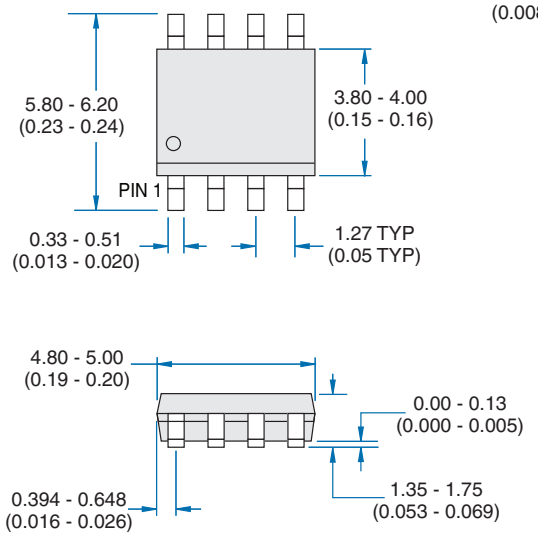
Recommended PCB Land Pattern

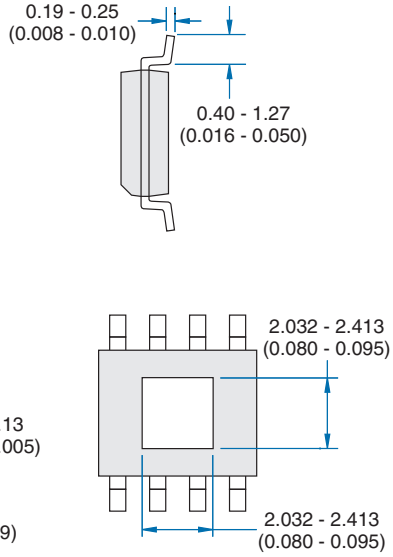


Dimensions
mm
(inches)

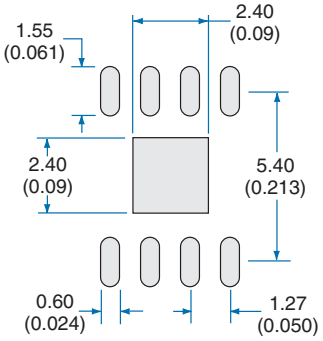
3.5.2 8-Pin SOIC EP Package

8-Pin SOIC Package with Exposed Thermal Pad





Recommended PCB Land Pattern

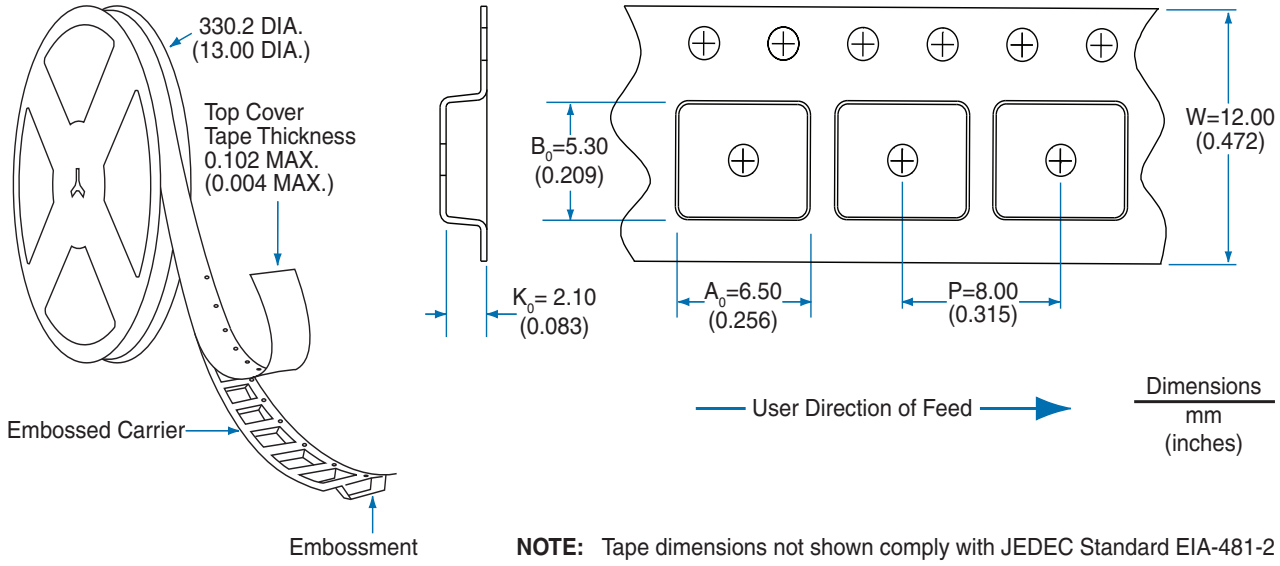


Dimensions
mm
(inches)

Note: Thermal pad should be electrically connected to GND, pin 3.

3.6 Packaging Information

For both the SOIC-8 and the SOIC-8 EP Packages.



NOTE: Tape dimensions not shown comply with JEDEC Standard EIA-481-2

For additional information please visit www.clare.com

Specifications: CPC9909 - R02

8/8/2011